REMARKS

Claims 1 through 25 are pending in this application.

I. Claim Rejections - 35 USC § 103

According to MPEP 706.02(j), the following establishes a *prima facie* case of obviousness under 35 U.S.C. §103:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

A. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozkan et al. (5933451), (hereinafter referred to as "Ozkan") in view of Kato (6271774). The Applicant respectfully traverses.

1. Regarding claim 1, the Examiner states that Ozkan fails to disclose the set-up input channel selection order as claimed, but that Kato teaches that prior art computing systems introduce long delay times when performing multiple calculations (Kato: column 6, lines 51-55). The Examiner explains that to help reduce this delay time, Kato discloses using a "set-up input channel selection order' (Kato: column 9, lines 1-15, wherein the set-up channel selection order is control signal), and therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to take the apparatus disclosed by Ozkan and add the selection order taught by Kato in order to obtain an apparatus that operates more efficiently by reducing the processing delay time.

However, Kato is teaching "aligned in order of decoding by the decoder" where the switch of encoder SW1 selects either a decoded picture from decoder or an external input picture from the controller. There is no actual teaching of storing according to a set-up input channel selection order.

The Federal Circuit has mentioned that "[t]he test for obviousness is not whether the features of one reference may be bodily incorporated into another reference...Rather, we look to see whether combined teachings render the claimed subject matter obvious." *In re Wood*, 599 F.2d 1032, 202 USPQ 171, 174 (CCPA 1979) (citing *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549-50 (CCPA 1969); *In re Mapelsden*, 329 F.2d 321, 322, 141 USPQ 30, 32 (CCPA 1964). Here, simply plugging in "a decoding order" into storing in frame buffer groups is not proper as there is no actual

teaching of storing the frame data into the frame buffer group corresponding to each channel in accordance with a setup input channel selection order. Having one reference possibly store data and the other having a decoding order does not mean that teaches of storing the frame data according to the setup input channel selection order.

In addition, decoding order is not the order in which the present invention is claiming as it states specifically that the storing is according to the set-up input channel selection order.

2. Ozkan and Kato also do not teach or suggest the channel data processor having the frame buffers storing the data with a separate encoder for then encoding the signals output from the channel data processor. In Ozkan, the channel data processor do not comprise the frame buffer, but the frame buffer is included in the encoder 14 which is part of bit rate allocator 30 as seen in figures 1-3. The Examiner clearly states that the processors are the processors in figures 1-3, but these do not comprise the frame buffer group.

B. Claims 3-14, 18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozkan et al. (5933451), (hereinafter referred to as "Ozkan") in view of Kato (6271774) in further view of Honda et al. (6493466), (hereinafter referred to as "Honda"). The Applicant respectfully traverses.

1. Regarding claims 3, 10, and 18, the Examiner that references teach two switches to connect the input channels, buffers, and output to encoders. The Examiner states that Honda teaches

that switches contacting the input channels with a buffer and switches contacting the frame buffer for outputting data to the encoder can precisely control an encoder (Honda: figure 5, wherein the first switch unit is switch 102, the second switch unit is switch 108/104, column 9, lines 22-47, wherein the precise control is the use of the switches to supply the data to the necessary locations). Therefore, the Examiner states that it would have been obvious to one having ordinary skill in the art at the time the invention was made to take the apparatus disclosed by Ozkan, add the selection order taught by Kato and add the switching units taught by Honda in order to obtain an apparatus that more precisely controls the compression of data.

However, the present claim states "multi-switch" units and Honda's figure 5 has only switches 104, 108 with a single on and off. Even switch 108 is a single and off that can be turned off with determination unit 107, but the signal when on only goes from input image memory 105 to the output 110 as mentioned in col. 9 of Honda. There is clearly no multi-switches and each switch is not capable of handling a plurality of input channels with the frame buffer group.

Moreover, there is no first multi-switch unit that selectively contacts each of the input channels with the frame buffer group. The switches 108 and 104 single on and off are not capable of selective contacts of each of the input channels of a plurality of input channels.

In addition the second multi-switch unit for selectively contacting with the frame buffer group is also not disclosed as the switches of Honda cannot selectively contact the different plurality of frame buffers of frame buffer group.

MPEP §706.02(j) strictly states that there must be a reasonable expectation of success and here the mere switches of Honda do give a reasonable expectation of success of forming the features

of the present invention.

One cannot even just state that the switches of Honda are multi-switches that be selectively contacted with because the here it is clear that the actual teachings of claim 3 are not taught or suggested and rather the Examiner is conjecturing that such multi-switches can be made based not on the prior art but by using the present invention as a blue-print for the rejection with is improper under 35USC§103.

Furthermore, merely taking switches from Honda and placing them in Ozkan is not enough to teach or suggest the features of the present invention. There must be an actual teaching or suggestion in the art. The switch 108 are from the input image memory to the compression encoder and 104 is from the reference image memory to the detector. The present invention on the other hand has the first multi-switch contacting each of the input channels and the second multi-switch selectively contacting with the frame buffer group. It is clear that Honda does not suggest such a connection of the switches and Ozkan teaches no such switches. Therefore, there is no actual teaching of the placement of the switches other than actually using the present invention as a blue-print for the rejection.

In addition one cannot just modify Honda into a multiplexer of Ozkan as the multiplexer of Ozkan 20 as Mux 20 does not deal with the frame buffer as seen in figure 1-3 as the data from the processors go to the bit rate allocator 30 as shown in figure 2 which is then to the encoder 14 which is shown in figure 3 having the frame buffer. Therefore, there is not teaching a multiple switch as

claimed.

2. Regarding claim 4, the Examiner states that Honda discloses "the first switch unit stores each unit of frame data in accordance with a set-up channel selection order, the second switch unit contacting with the frame buffer group in accordance with a set-up channel contact order and outputting the frame data"(Honda: column 9, lines 22-47, wherein the selection order is alternatively inputting the pictures between the two buffers).

However, as mentioned above, 102 and 108 of Honda are not multi-switches that are capable of manipulating a plurality of signals at the same time as is needed in dealing with multiple signals and there is no teaching or using the multiplexer of Ozkan for such purposes.

In addition, the second multi-switch unit does not actually contact with the frame buffer group as the MUX 20 of Ozkan contacts the processors and simple contacting input image memory as seen in switch 108 is not enough to teach of contacting the frame buffer group having a plurality of frame buffers. There must be an actual teaching or suggestion and the references here do not include such.

3. Regarding claims 6 and 12, the Examiner states that Honda discloses "a variable length encoder and outputting the encoded signals" (Honda: figure 17, item 1705) and "a parser for loading channel information about each frame and outputting the signals" (Honda: figure 17, column 17,

lines 60-65, wherein the parser is the synthesizing unit, the information about each frame is the information indicating that the image has not been skipped).

However, regarding the parser, it is not clear that Honda's synthesizing unit is related to the parser as it is not said to load channel information about each frame to signals output from the variable length encoder, and outputting signals. Rather, Honda only states that the synthesizing unit combines or synthesizes the coded data with information indicating that the image has been skipped. A parser separates out while a synthesizer combines and therefore, the synthesizing unit cannot be teaching the parser of the present invention.

4. Regarding claim 7, the Examiner states that Kato discloses "a channel selection unit including a key for setting up a select pattern in regard to the input channels" (Kato: column 9, lines 1-15, wherein the key for setting up a select pattern is the control signal) and "a channel controller for controlling the first and second switch unit in accordance with the select pattern" (Kato: column 9, lines 10-17).

However, column 9, lines 10-17 of Kato only mention a decoding order which does not teach or suggest a *key* included in the channel selection unit. Kato only states that the decoding order is directly supplied to an arithmetic part without passing a frame memory, motion predicting part and picture sequence rearranging part. There is no unit that actually sets up the pattern and has a key included for such pattern.

5. Regarding claim 9, the Examiner states to note the examiner's rejection for claim 1 and in

addition Honda discloses "encoding signals by using previous frame data stored in the prediction memory" (Honda: column 9, lines 44-52, wherein the compression encoder performs the encoding, the previous frame data is the second image).

However, Honda only describes a comparison between one image and another. However, there is no teaching or comparing frame data provided for each channel in a plurality of channels.

In addition, Honda and the other references fail to teach that the frame data is stored in a prediction memory for each and every corresponding channel. Honda for example only compares a single image with another. The step to compare for frame data for each channel is not actually taught or suggested.

6. Regarding claim 11, the Examiner states to note the examiner's rejection for claim 5 and in addition Honda discloses "a prediction memory selection unit for controlling prediction memory of channels corresponding to the selected channels by the second switch unit to be contracted between the adder and subtracter" (Honda: figure 17, wherein the controlling is performed by the motion amount detector).

However, as seen in paragraph 17 of Honda, the motion amount detector 1715 controls the switches 1714 and 1717 to perform or not perform encoding, but does not control the prediction memory selection unit for controlling the prediction memory of channels corresponding to selected specifically. Moreover, the switches 1714 and 1717 are not contacted between the adder and the subtracter as seen in figure 17 while the present invention does.

Respectfully, the Examiner must look at each and every claim limitation as required by MPEP 706.02(j) and here all the claimed limitations were not accounted for.

7. Regarding claims 13 and 22, the Examiner states to note the examiner's rejection for claim 7 and in addition Honda discloses "a channel controller for controlling the prediction memory" (Honda: figure 17, wherein the controlling is performed by the motion amount detector).

However, the motion amount detector 1715 of Honda in figure 17 does not control both the first and second multi-switch units and the prediction memory and such control is not according to the channel select pattern set up by the channel selection unit as seen in col. 17 of Honda.

8. Regarding claim 14, the Examiner states to note the examiner's rejection for claim 9 and in addition Honda discloses "selecting a prediction memory of channels corresponding to the input frame with numbers corresponding to the number of input channels" (Honda: figure 17, wherein the switch 1717 selects whether to engage the prediction memory or image memory).

However, the switch 1717 is not by engaging with memory teaching specifically selecting a prediction memory of channels corresponding to the input frame with numbers corresponding to the actual number of input channels. According to MPEP §706.02(j), the prior art reference (or references when combined) must teach or suggest all the claim limitations and here, the references do not teach all of the limitations and specifically all the limitations.

C. Claims 15-17, 19, 20-21, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozkan et al. (5933451), (hereinafter referred to as "Ozkan") in view of Kato (6271774) in further view of Honda et al. (6493466), (hereinafter referred to as "Honda") in further view of Faryar et al. (6625215), (hereinafter referred to as "Faryar"). The Applicant respectfully traverses.

1. Regarding claim 15, the Examiner states to note the examiners rejection for claims 1 and 3, and in addition claim 15 differs from claims 1 and 3 in that claim 15 further requires calculating a similarity between images, and Faryar teaches that prior art compression systems require a great overhead to be sent to the decoder (Faryar: column 1, lines 54-60.); to help alleviate this problem, Faryar discloses "an encoder for calculating a similarity by comparing image signals output from processor and previous frame data and selecting one mode set up differently for each other in regard to the present frame data in accordance with the calculated similarity" (figure 7, wherein the similarity is calculated from the comparison, column 6, lines 31-35, wherein the mode is the intra/inter mode); therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to take the apparatus disclosed by Ozkan, add the selection order taught by Kato, add the switching units taught by Honda, and add the similarity computing means taught by Faryar in order to obtain an apparatus that operates more efficiently by reducing computational overhead.

However, the inter difference mode and the intra difference modes are not selected according to the calculated similarity and encoding according to the selected encoding mode. No such teaching

or suggestion is actually made.

Moreover, the selection of one mode among a plurality of encoding modes is not in regard to the present frame data setup differently from each other in Faryar.

2. Regarding claim 19, Faryar discloses "an intra frame coder' (Faryar: figure 3, item 114), "and intra frame decoder" (Faryar: figure 3, item 116), "an adder" (Faryar: figure 3, item 132), "a subtracter" (Faryar: figure 3, item 126), and "a frame memory selection unit for controlling the frame memory of channels"' (Faryar: figure 3, items 112, 112A, 112B, 118, wherein the frame memory selection unit is the coding mode selector which controls the switches which controls the frame memory).

However, the frame memory selector unit does not control the memory channels to channels selected by the second multi-switch to be contacted between the adder and the subtracter as seen in figure 3 of Faryar.

3. Regarding claims 20 and 25, Faryar discloses "a similarity calculation unit calculating a similarity by comparing previous screen data and frame data of selected channel and determining an encoding mode with the macro block unit' (Faryar: figure 3, column 5, lines 46-50, wherein the previous screen data is the previously constructed sample, the mode is the inter/intra mode).

However, Faryar lacks a teaching of a set-up macro block unit as specifically stated in the claim as for example either figure 3 or col. 5 fails to mention such.

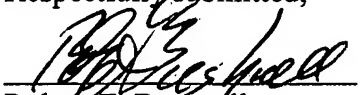
4. Regarding claims 21 and 23, Faryar discloses "determining a calculated similarity as the first mode when the calculated similarity is greater than a set-up reference value, and as the second mode when the calculated similarity is less than a set-up reference value" (Faryar: column 6, lines 31-35, wherein the set-up reference value is the inter/intra threshold, the two modes are the intra mode and the inter mode).

However, the threshold suggested in col. 6 is not a set-up reference value and col. 30 states that if the inter difference value is less then the intra then the interframe coding mode is made. There is no reference value to where there is comparison and then there is the selection of the mode, but the value of the inter and intra difference itself is compared instead in Faryar. As mentioned in MPEP 706.02(j), the prior art reference (or references when combined) must teach or suggest all the claim limitations and here it clear that not all the claimed limitations are taught or suggested.

In view of the foregoing remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. If there are any questions, the examiner is asked to contact the applicant's attorney.

No fee is incurred by this Response. Should there be a deficiency in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



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